What is claimed is:

1. A serial access memory comprising:

a first memory array including a plurality of first memory cells, a plurality of first sense amplifiers and a plurality of pairs of first bit lines connected to the first memory cells and the first sense amplifiers;

a second memory array including a plurality of second memory cells, a plurality of second sense amplifiers and a plurality of pairs of second bit lines connected to the second memory cells and the second sense amplifiers;

a plurality of pairs of column lines each of which is connected to one of the pairs of first bit lines and one of the pairs of the second bit lines;

a plurality of write registers each of which is connected to one of the pairs of column lines;

a write address accessing circuit connected to said write registers for selecting one of said write registers;

a plurality of read registers each of which is connected to one of the pairs of column lines;

a read address accessing circuit connected to said read registers for selecting one of said read registers;

an input circuit connected to said write registers; and

an output circuit connected to said read registers.

2. A serial access memory according to claim 1, further comprising,

a first X address accessing circuit connected to the first memory cells in a direction substantially perpendicular to the first bit lines, and

a second X address accessing circuit connected to the second memory cells in a direction substantially perpendicular to the second bit lines.

3. A serial access memory according to claim 1, further comprising,

a plurality of additional read registers each of which is connected to one of the pairs of column lines,

an additional read address accessing circuit connected to said additional read registers for selecting one of said read registers, and

an additional output circuit connected to said additional read registers.

4. A serial access memory according to claim 1, further comprising,

a plurality of first transfer circuits each of which is connected between one of said pairs of column lines and one of said pairs of first bit lines, said first transfer circuits connecting said column lines to said first bit lines in response to a first control signal, and

a plurality of second transfer circuits each of which is connected between one of said pairs of column lines and one of said pairs of second bit lines, said second transfer circuits connecting said column lines to said second bit lines in response to a second control signal.

5. A serial access memory according to claim 1, further comprising,

a plurality of third transfer circuits each of which is connected between one of said pairs of column lines and one of said read registers, said third transfer circuits connecting said column lines to said read registers in response to a third control signal, and

a plurality of fourth transfer circuits each of which is connected between one of said read registers and said output circuit, said fourth transfer circuits connecting said read registers to said output circuit in response to a

fourth control signal.

6. A serial access memory according to claim 1, further comprising,

a plurality of fifth transfer circuits each of which is connected between one of said pairs of column lines and one of said write registers, said fifth transfer circuits connecting said column lines to said write registers in response to a fifth control signal, and

a plurality of sixth transfer circuits each of which is connected between one of said write registers and said input circuit, said sixth transfer circuits connecting said write registers to said output circuit in response to a sixth control signal.

7. A serial access memory according to claim 1, wherein one of said read registers is connected to one column line of one of said pairs of column lines, and one of said write registers is connected to the other column line of one of said pairs of column lines.

8. A serial access memory comprising:

a first memory array including a plurality of first memory cells, a plurality of first sense amplifiers and a plurality of first and second pairs of bit lines connected to the first memory cells and the first sense amplifiers;

a second memory array including a plurality of second memory cells, a plurality of second sense amplifiers and a plurality of third and fourth pairs of bit lines connected to the second memory cells and the second sense amplifiers;

a plurality of pairs of first column lines each of which is connected to one of the first pairs of bit lines and one of the third pairs of the bit lines;

a plurality of pairs of second column lines each of which is connected to one of the second pairs of bit lines and one of the fourth pairs of the bit lines;

a plurality of write registers;

a plurality of first transfer circuits each of which is connected between one of said first column lines to one of said write registers, said first transfer circuits connecting the first column lines to said write registers in response to a first control signal;

a plurality of second transfer circuits each of which is connected

between one of said second column lines to one of said write registers, said second transfer circuits connecting the second column lines to said write registers in response to a second control signal;

a write address accessing circuit connected to said write registers for selecting one of said write registers;

a plurality of read registers;

a plurality of third transfer circuits each of which is connected between one of said first column lines to one of said read registers, said third transfer circuits connecting the first column lines to said read registers in response to a third control signal;

a plurality of fourth transfer circuits each of which is connected between one of said second column lines to one of said read registers, said fourth transfer circuits connecting the second column lines to said read registers in response to a fourth control signal;

a read address accessing circuit connected to said read registers for selecting one of said read registers;

an input circuit connected to said write registers; and

an output circuit connected to said read registers.

9. A serial access memory according to claim 8, further comprising,

a first X address accessing circuit connected to the first memory cells in a direction substantially perpendicular to said first and second pairs of bit lines, and

a second X address accessing circuit connected to the second memory cells in a direction substantially perpendicular to said third and fourth pairs of bit lines.

10. A serial access memory according to claim 8, wherein each of said write registers and read registers is located between one of said first column lines.

11. A serial access memory according to claim 8, further comprising,

a plurality of fifth transfer circuits each of which is connected between one of said pairs of first column lines and one of said pairs of first bit lines, said fifth transfer circuits connecting said column lines to said first bit

lines in response to a fifth control signal,

a plurality of sixth transfer circuits each of which is connected between one of said pairs of first column lines and one of said pairs of third bit lines, said sixth transfer circuits connecting said third column lines to said third bit lines in response to a sixth control signal.

12. A serial access memory according to claim 8, further comprising,

a plurality of seventh transfer circuits each of which is connected between one of said pairs of second column lines and one of said pairs of second bit lines, said seventh transfer circuits connecting said second column lines to said second bit lines in response to a seventh control signal,

a plurality of eighth transfer circuits each of which is connected between one of said pairs of second column lines and one of said pairs of fourth bit lines, said eighth transfer circuits connecting said second column lines to said fourth bit lines in response to an eighth control signal.

13. A serial access memory according to claim 8, further

comprising,

a plurality of ninth transfer circuits each of which is connected between one of said input circuit and one of said write registers, said ninth transfer circuits connecting said input circuit to said write registers in response to a ninth control signal, and

a plurality of tenth transfer circuits each of which is connected between said output circuit and one of said read registers, said tenth transfer circuits connecting said output circuit to said read registers in response to a tenth control signal.

14. A serial access memory comprising:

a first memory array including a plurality of first memory cells, a plurality of first sense amplifiers and a plurality of first and second pairs of bit lines connected to the first memory cells and the first sense amplifiers;

a second memory array including a plurality of second memory cells, a plurality of second sense amplifiers and a plurality of third and fourth pairs of bit lines connected to the second memory cells and the second sense amplifiers;

a plurality of pairs of column lines each of which is connected to one of said first pairs of bit lines, one of said second pairs of bit lines, one of said third pairs of bit lines and one of said fourth pairs of bit lines;

a plurality of first transfer circuits each of which is connected between one of said column lines to one of said first pairs of bit lines, said first transfer circuits connecting the column lines to said first pairs of bit lines in response to a first control signal;

a plurality of second transfer circuits each of which is connected between one of said column lines to one of said second pairs of bit lines, said first transfer circuits connecting the column lines to said second pairs of bit lines in response to a second control signal;

a plurality of third transfer circuits each of which is connected between one of said column lines to one of said third pairs of bit lines, said first transfer circuits connecting the column lines to said third pairs of bit lines in response to a third control signal;

a plurality of fourth transfer circuits each of which is connected between one of said column lines to one of said fourth pairs of bit lines, said first transfer circuits connecting the column lines to said fourth pairs of bit lines

in response to a fourth control signal;

a plurality of write registers;

a write address accessing circuit connected to said write registers for selecting one of said write registers;

a plurality of read registers;

a read address accessing circuit connected to said read registers for selecting one of said read registers;

an input circuit connected to said write registers; and

an output circuit connected to said read registers.

15. A serial access memory according to claim 14, further comprising,

a first X address accessing circuit connected to the first memory cells in a direction substantially perpendicular to the first and second bit lines, and

a second X address accessing circuit connected to the second memory cells in a direction substantially perpendicular to the third and fourth bit lines.

16. A serial access memory according to claim 14, wherein each of said write registers and read registers is located between one of said pairs of column lines.

17. A serial access memory according to claim 14, further comprising,

a plurality of fifth transfer circuits each of which is connected between one of said input circuit and one of said write registers, said fifth transfer circuits connecting said input circuit to said write registers in response to a fifth control signal, and

a plurality of sixth transfer circuits each of which is connected between said output circuit and one of said read registers, said sixth transfer circuits connecting said output circuit to said read registers in response to a sixth control signal.

18. A serial access memory according to claim 14, further comprising,

a plurality of seventh transfer circuits each of which is connected

between one of said pairs of column lines and one of said write registers, said seventh transfer circuits connecting said column lines to said write registers in response to a seventh control signal, and

a plurality of eighth transfer circuits each of which is connected between said pairs of column lines and one of said read registers, said eighth transfer circuits connecting said column lines to said read registers in response to an eighth control signal.

19. A serial access memory according to claim 14, further comprising a division circuit connected to said column lines, said division circuit electrically dividing said first memory array from said second memory array in response to a divisional signal.